

Packet dispatching schemes supporting uniform and nonuniform traffic distribution patterns in MSM Clos-network switches

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Abstract—In this paper new packet dispatching schemes for efficient support of the uniform as well as the nonuniform traffic distribution patterns in Memory-Space-Memory (MSM) Clos-network switches are presented. Three such schemes, called Static Dispatching-First Choice (SD-FC), Static Dispatching-Optimal Choice (SD-OC) and Input Module (IM)-Output Module (OM) Matching (IOM), are proposed and evaluated. The algorithms are able to unload the overloaded input buffers employing a central arbiter. This effect is a desirable feature especially for effective support of the nonuniform traffic distribution patterns. We show via simulation that the proposed schemes deliver very good performance in terms of throughput, cell delay, and input buffers size under different traffic distribution patterns. The results obtained for the proposed algorithms are compared with the results obtained for selected request-grant-accept iterative packet dispatching schemes.

Index Terms—Clos-network, packet scheduling, packet switching, virtual output queuing.

I. INTRODUCTION

THE switching fabric in high-performance packet switching nodes may be built as a single stage-switch (e.g. crossbar) or a multi-stage switch, such as the Clos switching fabric. The switching process in a multi-stage switching fabric consists of two activities, namely input-output matching and route assignment between the first and last stages. These two phases can be processed separately or simultaneously. Since the high-speed switching fabrics support fixed-length packets called cells, packets of variable size must be segmented into cells at switch input ports, and cells must be reassembled into packets at switch output ports [1].

While cells are being routed in a switching fabric, it is very likely that more than one cell is destined for the same output port or for a physical link inside the multi-stage switching fabric. Cells that have lost contention must be either discarded or buffered. Buffers may be placed at inputs, outputs, inputs and outputs, and/or within the switching fabric [2]. The virtual output queuing (VOQ) is widely implemented as a good solution for input queued (IQ) switches, to avoid the Head-Of-Line (HOL) blocking problem encountered in the input-buffered switches. In VOQ switches every input provides a single and separate FIFO for each output. Such a FIFO is called a Virtual Output Queue. When a new cell arrives at the input port, it is stored in the destined queue and waits for transmission through a switching fabric. To solve internal blocking and output port contention problems in VOQ

switches, fast arbitration schemes are needed. The arbitration scheme decides which items of information should be passed from inputs to arbiters, and – based on that decision – how each arbiter picks one cell from among all input cells destined for the output. Algorithms which can assign the route between input and output modules are usually called packet dispatching schemes. Considerable work has been done on scheduling algorithms for VOQ switches. Most of them achieve 100% throughput under uniform traffic, but the throughput is usually reduced under nonuniform traffic [1], [3]–[14]. A switch can achieve 100% throughput under uniform or nonuniform traffic if the switch is stable, as was defined in [15]. In general, a switch is stable for a particular arrival process if the expected length of the input queues does not grow without limits.

Multiple-stage Clos-network switches are a potential solution to overcome the limited scalability of single-stage switches, in terms of the number of I/O chip pins and the number of switching elements. Different dispatching schemes for the three-stage Clos-network switches were proposed in the literature [4]–[6], [9]–[14]. The basic idea of these algorithms is to use the effect of desynchronization of arbitration pointers and a common request-grant-accept handshaking scheme. All high speed switching fabrics implemented by the manufacturers of switches/routers are now based on SERDES technology. The signals passing through these serial links are within the range of several hundred nanoseconds. It is very difficult to implement the algorithms with multiple-phase iterations in a three-stage environment with currently available technologies, because of time constraints (one slot time in a 10 Gbps switching fabric lasts around 50 ns).

In this paper SD-FC, SD-OC, and IOM packet dispatching schemes are presented. These algorithms give better performance results than other dispatching schemes proposed for the MSM Clos switching fabric, and can achieve 100% throughput for both the uniform and the nonuniform traffic distribution patterns. The remainder of this paper is organized as follows. Section II introduces some background knowledge concerning the MSM Clos switching fabric that we refer to throughout this paper. Section III presents the SD-FC, SD-OC, and IOM packet dispatching schemes. Section IV is devoted to performance evaluation of the proposed algorithms. The comparison of cell delay between proposed algorithms and the selected multiple-phase iterative packet dispatching schemes is also shown. We conclude this paper in Section V.

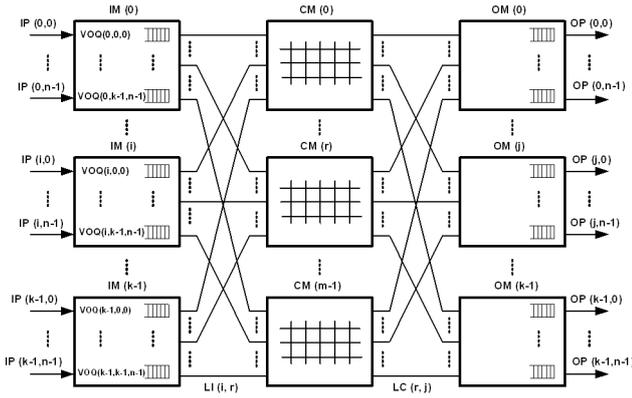


Fig. 1. The MSM Clos switching fabric architecture.

II. MSM CLOS SWITCHING NETWORK

Clos-networks are well known and widely analyzed in the literature [16]. The three-stage Clos-network architecture is denoted by $C(m, n, k)$, where parameters m , n , and k entirely determine the structure of the network. We define the MSM Clos switching fabric based on the terminology used in [4] (see Fig. 1).

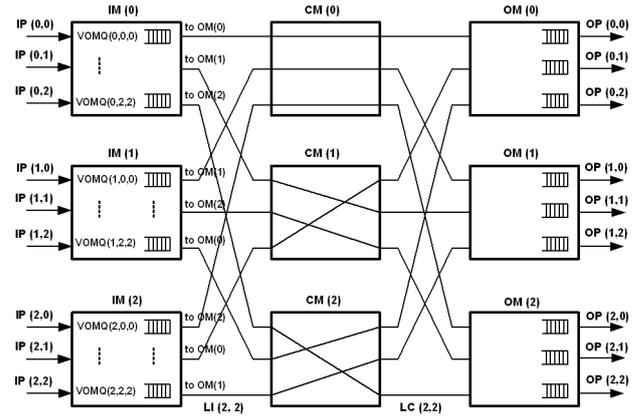
In the MSM Clos switching fabric architecture the first stage consists of k IMs, and each of them has an $n \times m$ dimension and nk $VOQ(i, j, h)$ to eliminate Head-Of-Line blocking. The second stage consists of m bufferless CMs, and each of them has a $k \times k$ dimension. The third stage consists of k OMs of capacity $m \times n$, where each $OP(j, h)$ has an output buffer. Each output buffer can receive at most m cells from m CMs, so a memory speedup is required here.

Generally speaking, in the MSM Clos switching fabric architecture each $VOQ(i, j, h)$ located in $IM(i)$ stores cells going from $IM(i)$ to the $OP(j, h)$ at $OM(j)$. In one cell time slot VOQ can receive at most n cells from n input ports and send one cell to any CMs. A memory speedup of n is required here because the rate of memory work has to be n times higher than the line rate. Each $IM(i)$ has m output links $LI(i, r)$ connected to each $CM(r)$, respectively. A $CM(r)$ has k output links $LC(r, j)$ which are connected to each $OM(j)$, respectively.

In simulation experiments we consider the Clos switching fabric without any expansion, denoted by $C(n, n, n)$, so in the description of the packet dispatching schemes in Section III, parameters k and m are not used. We also use Virtual Output Module Queues (VOMQs), instead of VOQs. In this case, an input buffer in each IM is divided into k parallel queues, each of them storing cells destined for different OMs. It is possible to arrange buffers in such way because OMs are nonblocking. Memory speedup of n is necessary here. There are fewer queues in each IM but they are longer than VOQs. Each $VOMQ(i, j)$ stores cells going from $IM(i)$ to the $OM(j)$.

III. PACKET DISPATCHING SCHEMES

Under the nonuniform traffic distribution patterns, selected VOQs store more cells than others. Because of that, it is

Fig. 2. Static connection patterns in CMs, $C(3, 3, 3)$.

necessary to implement a special mechanism for a packet dispatching scheme, which is able to send up to n cells from $IM(i)$ to $OM(j)$ in the same time slot, in order to unload overloaded buffers. Three dispatching schemes presented in this paper have such possibility.

The proposed packet dispatching schemes perform matching between each IM and OM, taking into account the number of cells waiting in VOMQs. Each VOMQ has its own counter $PV(i, j)$ which shows the number of cells destined for $OM(j)$. The value of $PV(i, j)$ is increased by 1 when a new cell is written into memory, and decreased by 1 when the cell is sent out to $OM(j)$. The algorithms use the central arbiter to indicate the matched pairs of $IM(i) - OM(j)$ but the set of data sent to the arbiter by each scheme is different. Therefore, the architecture and functionality of each arbiter is also different. After matching phase, in the next time slot $IM(i)$ is allowed to send up to n cells to the selected $OM(j)$.

In the SD-OC and SD-FC schemes the central arbiter matches $IM(i)$ and $OM(j)$ only if the number of cells buffered in $VOMQ(i, j)$ is at least equal to n . Under the nonuniform traffic distribution patterns this happens very often, contrary to the uniform traffic distribution. In the proposed packet dispatching schemes, each VOMQ has to wait until at least n cells are stored before being allowed to make a request. To reduce latency and avoid starvation, a very simple packet dispatching routine, called Static Dispatching (SD), is also used. Under this algorithm, connecting paths in the MSM Clos switching fabric are set up according to connection patterns which are static but different in each CM (see Fig. 2). These fixed connection paths between IMs and OMs eliminate the handshaking process with the second stage, and no internal conflicts in the switching fabric will occur. Also, no arbitration process is necessary. Cells destined for the same OM, but located in different IMs, will be sent through different CMs. In detail, the SD algorithm works as follows:

Step 1: According to the connection pattern of $IM(i)$, match all output links $LI(i, r)$ with cells from VOMQs.

Step 2: Send the matched cells in the next time slot. If there is any unmatched output link, it remains idle.

The SD-OC and SD-FC schemes are very similar but the central arbiter which matches the IMs and OMs works in

a different way. In both algorithms the $PV(i, j)$ counter which reaches the value equal to or greater than n sends the information about an overloaded buffer to the central arbiter. In the central arbiter there is a binary matrix of VOMQ buffers load. If the value of matrix element $x[i, j] = 1$, it means that $IM(i)$ has at least n cells that should be sent to $OM(j)$.

In the SD-OC scheme the main task of the central arbiter is to find an optimal set of 1s in the matrix. The best case is n 1s but it is possible to choose only one 1 from column i and row j . If there is no such set of 1s, the arbiter tries to find a set of $n - 1$ 1s which fulfill the same conditions, and so on. The round-robin routine is used for the starting point of the searching process. Otherwise, the MSM Clos switching fabric works under the SD scheme.

The main difference between the SD-OC and SD-FC lies in the operation of the central arbiter. In the SD-FC scheme the central arbiter does not look for an optimal set of 1s but tries to match $IM(i)$ with $OM(j)$, choosing the first 1 found in column i and row j . No optimization process for selecting the IM-OM pairs is employed. In detail, the SD-OC algorithm works as follows:

Step 1: If the value of the $PV(i, j)$ counter is equal to or greater than n , send a request to the central arbiter.

Step 2: If the central arbiter receives the request from $IM(i)$, it sets the value of the buffer load matrix element $x[i, j]$ to 1 (the values of i and j come from the counter $PV(i, j)$).

Step 3: After receiving all requests, the central arbiter tries to find an optimal set of 1s which allows the greatest number of cells to be sent from IMs to OMs. The central arbiter has to go through all rows of the buffer load matrix to find a set of n 1s representing $IM(i) - OM(j)$ matching. If it is not possible to find a set of n 1s, it attempts to find a set of $(n - 1)$ 1s, and so on.

Step 4: In the next time slot send n cells from IMs to the matched OMs. Decrease the value of $PV(i, j)$ by n . For the IM-OM pairs not matched by the central arbiter, use the SD scheme and decrease the value of PV counters by 1.

The steps in the SD-FC scheme are very similar to the steps in the SD-OC scheme but the optimization process in the third step is not carried out. The central arbiter chooses the first 1 which fulfills the requirements in each row. The row searched as the first one is selected according to the round-robin routine.

The IOM packet dispatching scheme also employs the central arbiter to make a match between each IM and OM. The cells are sent only between IM-OM pairs matched by the arbiter. The SD scheme is not used. In detail, the IOM algorithm works as follows:

Step 1 (each IM): Sort the values of $PV(i, j)$ in descending order. Send a request to the central arbiter, containing a list of the OMs identifiers. The identifier of $OM(j)$ for which $VOMQ(i, j)$ stores the greatest number of cells should be placed on the list as the first one, and the identifier of $OM(s)$ for which $VOMQ(i, s)$ stores the smallest number of cells should be placed on the list as the last one.

Step 2 (central arbiter): The central arbiter analyzes the request received from $IM(i)$ and checks whether it is possible to match this IM with $OM(j)$ whose identifier was sent as the

first one on the list in the request. If matching is not possible because the $OM(j)$ was matched with other IM, the arbiter selects the next OM on the list. The round-robin arbitration is employed for the selection of $IM(i)$ for which the request is analyzed as the first one.

Step 3 (central arbiter): The central arbiter sends confirmation to each IM with the identifier of $OM(t)$ to which the IM is allowed to send cells.

Step 4 (each IM): Match all output links $LI(i, r)$ with cells from $VOMQ(i, t)$. If there are less than n cells to be sent to $OM(t)$, some output links remain unmatched.

Step 5 (each IM): Decrease the value of $PV(i, t)$ by the number of cells to be sent to $OM(t)$.

Step 6 (each IM): In the next time slot send the cells from the matched $VOMQ(i, t)$ to the $OM(t)$ selected by the central arbiter.

IV. SIMULATION EXPERIMENTS

A. Packet arrival models

Two packet arrival models are considered in simulation experiments: the Bernoulli arrival model and the bursty traffic model. In the Bernoulli arrival model, cells arrive at each input in a slot-by-slot manner. Under the Bernoulli arrival process, the probability that there is a cell arriving in each time slot is identical to and independent of all other slots. The probability that a cell may arrive in a time slot is denoted by p and is referred to as the load of the input. In the bursty traffic model, each input alternates between active and idle periods. During active periods, cells destined for the same output arrive continuously in consecutive time slots. The average burst (active period) length is set to 10 cells.

B. Traffic distribution models

We consider several traffic distribution models which determine the probability that a cell which arrives at an input will be directed to a certain output. The considered traffic models are:

Uniform traffic. This type of traffic is the most commonly used traffic profile. In uniformly distributed traffic, the probability p_{ij} that a packet from input i will be directed to output j is uniformly distributed through all outputs, that is:

$$p_{ij} = p/N \quad \forall i, j. \quad (1)$$

Trans-diagonal traffic. In this traffic model some outputs have a higher probability of being selected, and respective probability p_{ij} was calculated according to the following equation:

$$p_{ij} = \begin{cases} \frac{p}{2} & \text{for } i = j \\ \frac{p}{2(N-1)} & \text{for } i \neq j. \end{cases} \quad (2)$$

Bi-diagonal traffic. This type of traffic is very similar to the trans-diagonal traffic but packets are directed to one of two outputs, and respective probability p_{ij} was calculated according to the following equation:

$$p_{ij} = \begin{cases} \frac{2}{3}p & \text{for } i = j \\ \frac{p}{3} & \text{for } j = (i + 1) \pmod{N} \\ 0 & \text{otherwise.} \end{cases} \quad (3)$$

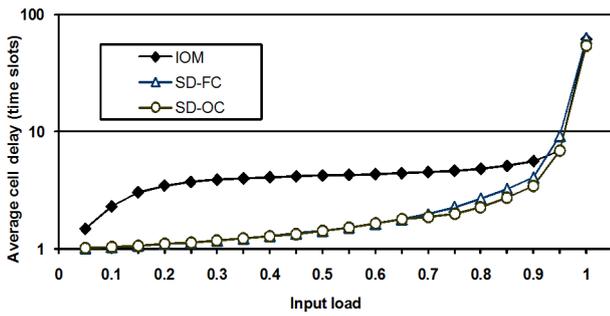


Fig. 3. Average cell delay, uniform traffic.

Chang's traffic. This model is defined as:

$$p_{ij} = \begin{cases} 0 & \text{for } i = j \\ \frac{p}{N-1} & \text{otherwise.} \end{cases} \quad (4)$$

C. Results of simulation experiments

The experiments have been carried out for the MSM Clos switching fabric of size $64 \times 64 - C(8, 8, 8)$, and for a wide range of traffic loads per input port: from $p = 0.05$ to $p = 1$, with a step of 0.05. The 95% confidence intervals that have been calculated after t -student distribution for ten series with 50000 cycles (after the starting phase comprising 15000 cycles, which enables the stable state of the switching fabric to be reached) are at least one order lower than the mean value of the simulation results, and, therefore, they are not shown in the figures. We have evaluated two performance measures: average cell delay in time slots and maximum VOMQs size (we have investigated the worst case). The size of the buffers at the input and output side of switching fabric is not limited, so cells are not discarded. However, they encounter delay instead. Because of the unlimited size of buffers, no mechanism controlling flow control between the IMs and OMs (to avoid buffer overflows) is implemented. The results of the simulation are shown in the charts (Fig. 3, Fig. 4, Fig. 5, Fig. 6, Fig. 7, Fig. 8, Fig. 9, Fig. 10, Fig. 11, Fig. 12). Fig. 3, Fig. 5, Fig. 7, Fig. 9, and Fig. 11 show the average cell delay in time slots obtained for the uniform, trans-diagonal, bi-diagonal, Chang's, and bursty traffic patterns, whereas Fig. 4, Fig. 6, Fig. 8, Fig. 10 and Fig. 12 show the maximum VOMQ size in the number of cells. Fig. 11 and Fig. 12 show the results for the bursty traffic with average burst size $b = 10$ (10 is the number of cells).

We can see that the MSM Clos switching fabric with all the schemes proposed has 100% throughput for all kinds of investigated traffic distribution patterns and for the bursty traffic. The average cell delay is less than 10 for a wide range of input loads, regardless of the traffic distribution pattern. It is a very interesting result especially for the trans-diagonal and the bi-diagonal traffic patterns. Both traffic patterns are highly demanding and many packet dispatching schemes proposed in the literature cannot provide 100% throughput for the investigated switching fabric. For the bursty traffic, the average cell delay becomes very similar to a linear function of input load with the maximum value less than 150. We can see

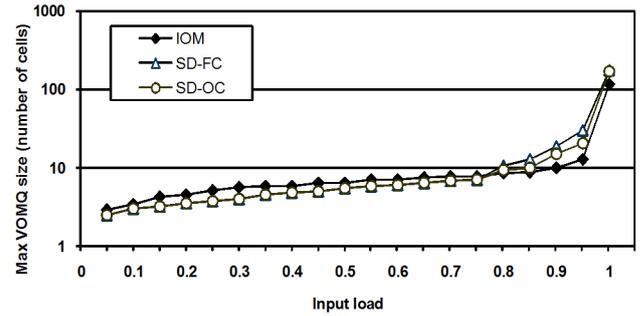


Fig. 4. The maximum VOMQ size, uniform traffic.

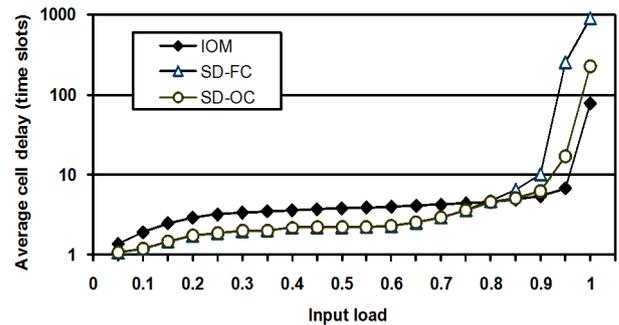


Fig. 5. Average cell delay, trans-diagonal traffic.

that the very complicated arbitration routine used in the SD-OC scheme does not improve the performance of MSM Clos switching fabric. In some cases the results are even worse than for the IOM scheme (the trans-diagonal traffic with very high input load and bursty traffic). Generally, the IOM scheme gives higher latency than the SD schemes, especially for low to medium input load. This is due to matching $IM(i)$ to that $OM(j)$ to which it is possible to send the greatest number of cells. As a consequence, it is less probable that IM-OM pairs will be matched to serve one, two, or three cells per cycle.

The size of VOMQ in the MSM Clos switching network depends on the traffic distribution pattern. For all proposed packet distribution schemes and uniform and Chang's traffic the maximum size of VOMQ is less than 140 cells. This means that in the worst case the average number of cell waiting for transmission to a particular output was not bigger than 16. For the trans-diagonal traffic and the IOM scheme the maximum size of VOMQ is less than 200 but for SD-OC and SD-FC the sizes are greater and reach 700 and 3000, respectively. For the bi-diagonal traffic the smallest size of VOMQ was obtained for the SD-OC scheme for which it was less than 290. For the bursty traffic the maximal size of VOMQ reaches 750 for SD-FC, 500 for SD-OC, and 350 for the IOM scheme.

D. Comparison of cell delay between proposed schemes and selected multiple-phase packet dispatching algorithms

The primary multiple-phase dispatching algorithms for the buffered Clos-network switches were proposed in [4]. The basic idea of these algorithms is to use the effect of desynchronization of arbitration pointers in the Clos-network switch and

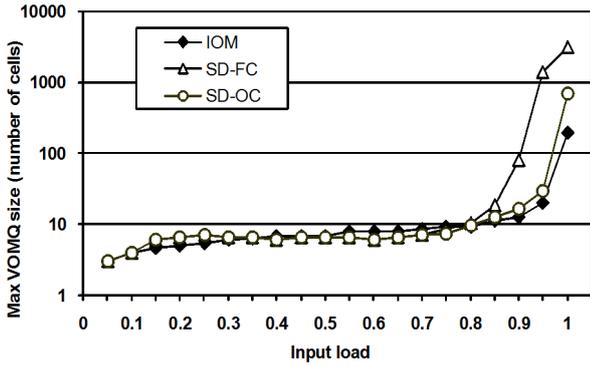


Fig. 6. The maximum VOMQ size, trans-diagonal traffic.

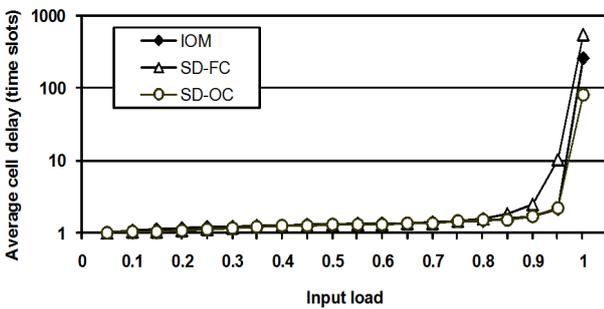


Fig. 7. Average cell delay, bi-diagonal traffic.

the common request-grant-accept handshaking scheme. The well known algorithm with multiple-phase iterations is the CRRD (*Concurrent Round-Robin Dispatching*). Other algorithms like the CMSD (*Concurrent Master-Slave Round-Robin Dispatching*) [4], SRRD (*Static Round-Robin Dispatching*) [6], and, as proposed by us in [11], CRRD-OG (*Concurrent Round-Robin Dispatching with Open Grants*) use the main idea of the CRRD scheme and try to improve the results by implementing different mechanisms.

Fig. 13, Fig. 14, Fig. 15 show the comparison between average cell delays obtained for the CRRD, CMSD, SRRD, and CRRD-OG schemes with four iterations (more than $n/2$ iterations do not change the performance of all investigated iterative schemes significantly) and average cell delay obtained for the schemes proposed in this paper. The simulation experiments were carried out for all kinds of investigated traffic distribution patterns, but only results for the uniform, trans-diagonal, and bi-diagonal traffic patterns are shown. The conditions of computer simulation experiments were the same for all investigated schemes.

For the uniform traffic distribution pattern all schemes can achieve 100% throughput. The best results can be obtained by using the CRRD-OG scheme, but the results are almost the same as for SD schemes. For highly demanding traffic distribution patterns like the trans-diagonal and bi-diagonal ones, only SD-FC, SD-OC, and IOM schemes can provide 100% throughput for the MSM Clos switching fabric. The investigated request-grant-accept packet dispatching schemes are not able to provide such high efficiency. The best results

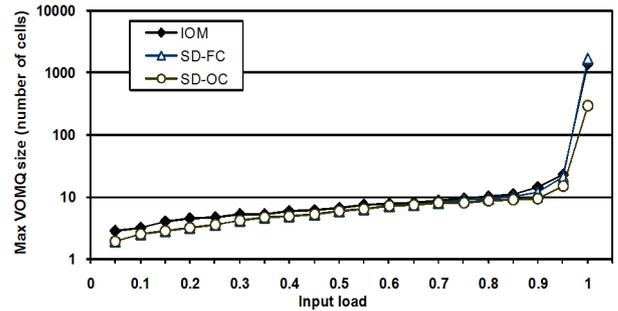


Fig. 8. The maximum VOMQ size, bi-diagonal traffic.

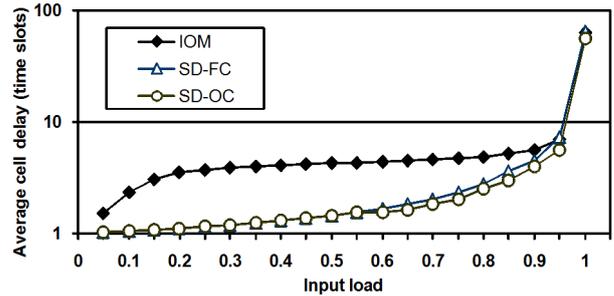


Fig. 9. Average cell delay, Chang's traffic.

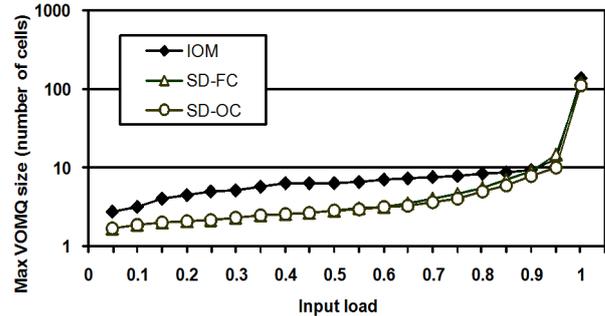


Fig. 10. The maximum VOMQ size, Chang's traffic.

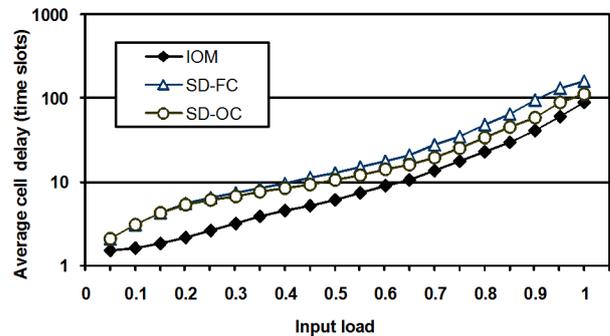


Fig. 11. Average cell delay, bursty traffic.

from among multiple-phase algorithms have been obtained for the CRRD-OG scheme. These are respectively: under the trans-diagonal traffic pattern: 85% throughput for four iterations (Fig. 14), and under the bi-diagonal traffic pattern, 95% (Fig. 15).

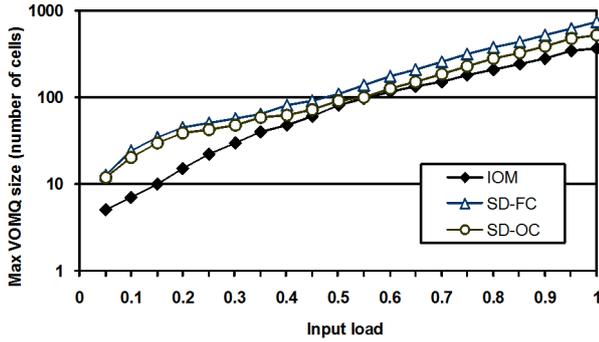


Fig. 12. The maximum VOMQ size, bursty traffic.

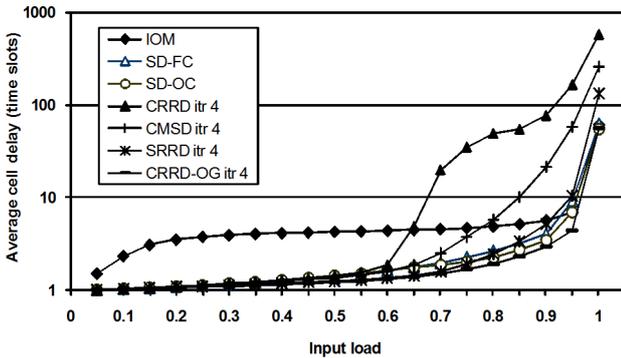


Fig. 13. Average cell delay for selected request-grant-accept algorithms (four iterations) and the proposed schemes, uniform traffic.

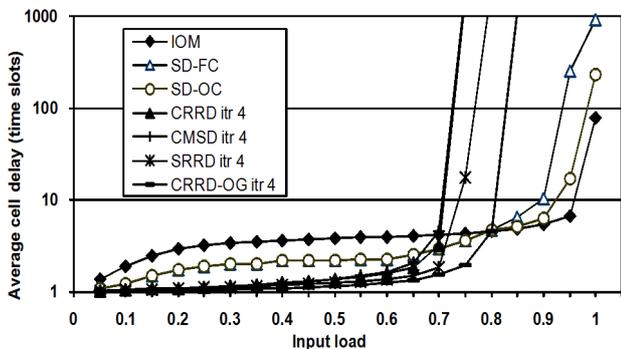


Fig. 14. Average cell delay for selected request-grant-accept algorithms (four iterations) and the proposed schemes, trans-diagonal traffic.

The investigated request-grant-accept packet dispatching schemes are based on the effect of desynchronization of arbitration pointers in the Clos-network switch. We have made an attempt to improve the desynchronization method for the CRRD-OG scheme to ensure 100% throughput for the nonuniform traffic distribution patterns. Additional pointers and arbiters for open grants were added to the MSM Clos switching fabric but the scheme was not able to provide 100% throughput for the nonuniform traffic distribution patterns. To the best of our knowledge, it is not possible to achieve very good desynchronization of pointers using the methods implemented in the iterative packet dispatching schemes. In our opinion, the decisions of distributed arbiters have to be

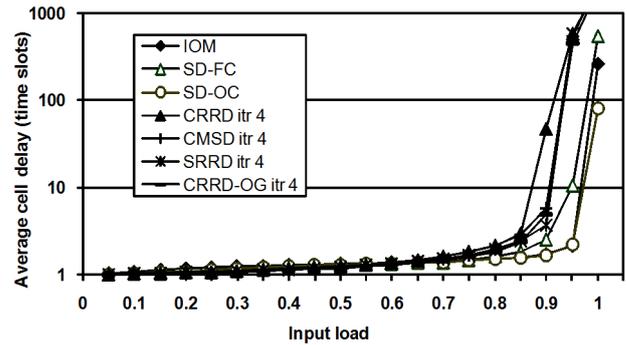


Fig. 15. Average cell delay for selected request-grant-accept algorithms (four iterations) and the proposed schemes, bi-diagonal traffic.

supported by the central arbiter but the implementation of such solutions in the real equipment will be very complex. Therefore the algorithms, which are able to unload the overloaded input buffers like SD-FC and IOM should be implemented.

V. CONCLUSION

We have proposed the SD-FC, SD-OC, and IOM packet dispatching schemes for the MSM Clos switching fabric. The algorithms employ the central arbiter to match IMs with OMs. In SD-FC and IOM schemes the arbiter performs relatively simple functions. Simulation experiments have shown that the proposed schemes are very promising and give very good results for both the uniform and nonuniform traffic distribution patterns. The algorithms can manage all investigated traffic patterns very effectively, providing 100% throughput. This is a highly desirable property of the packet dispatching algorithm for the switching fabric of the next generation packet node. A hardware implementation of the central arbiters required by the proposed schemes will be subject to further research.

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The main area of interest of the author covers packet dispatching and scheduling algorithms for both electronic and optical switching fabrics.