Bit Error Rate Tester for 10 Gb/s Fibre Optic Link

Łukasz Śliwczyński and Przemysław Krehlik

Abstract—The bit error rate tester suitable for operation in 10 Gb/s fibre optic links is described in the paper. The BER tester was built from commercially available components. Generation and reception of 10 Gb/s data stream is performed with help of high-speed serialiser and deserialiser by Maxim. The main functions of the BER tester are implemented in the field programmable gate array (FPGA) Spartan3 device by Xilinx. The part of the FPGA runs with the clock speed equal to 622 MHz. Some measurement results obtained in the fibre optic links operated with 10 Gb/ data rate are also presented.

Index Terms—bit error rate, fibre optic links, field programmable gate arrays

I. INTRODUCTION

BIT error rate (BER) is one of the most important parameters describing the performance of transmission in the digital link. It is usually defined as:

$$BER = \frac{n_e}{N},\tag{1}$$

where n_e is the total number of received bits and N is the number of bits being in error. Because of random nature of the phenomenon, BER is also regarded as the probability of errors occurring during data transmission. BER in the order of 10^{-9} or even 10^{-12} is often considered as being characteristic for modern fibre optic systems. Because of that, measuring BER accordingly to equation (1) is inconvenient as it would require using a counter with huge capacity (generally, greater than 1/BER). Thus, it is better to transform equation (1) into:

$$BER = \frac{1}{B} \frac{n_e}{\Delta t},\tag{2}$$

where B is the bit rate and Δt is the measurement time. When using equation (2), it is convenient to express Δt in seconds, and the bit rate is only a scaling factor.

Nowadays 10 Gb/s transmission rate is increasingly common in fibre optic links. Commercial BER testers capable of operation with such fast signals are often very advanced (e.g. [1]–[3]). They allow the testing of a transmission system more comprehensively (for example to check its immunity to jitter or pathological data patterns), not just to simply measure BER. Unfortunately, the cost of such test systems is very high, which make them rarely available for most universities research/students labs. Thus, an idea was born to develop 10 Gb/s BER tester (BERT), which would be possible to be built from commercially available components, with most of its functions being implemented in the FPGA circuit. Below a

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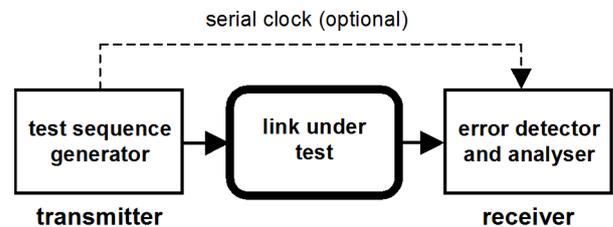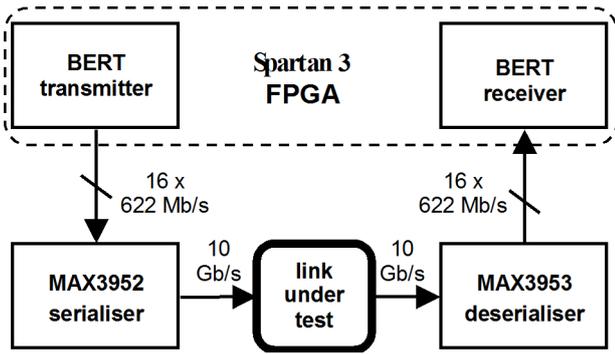
Fig. 1. Generic block diagram of the BER tester.

design of such BERT is presented, along with a theory of its operation.

II. IDEA OF OPERATION OF THE BER TESTER

Each BERT is composed of two main parts: the transmitter (that includes the generator of the test sequences) and the receiver (that includes the error detector and analyser) [4]. The block diagram of the BER tester is presented in Fig. 1.

The purpose of the test sequence generator is to produce the stream of the data bits according to some rule that must be known for the receiver as well. The most often the pseudo random bit sequence (PRBS) generators are used for this purpose. There are a number of standard polynomials defining different PRBS, developed by standardisation bodies (e.g. [5]) for testing telecommunication equipment. Alternatively, some bit sequence defined by the user and stored in the tester memory may be periodically generated.

In the receiver, the error detector compares the received bits with the original pattern and, in case of incompatibility, increases the error counter. The result of the measurement may be presented in many different ways: simply as a number, or in the form of detailed diagram, displaying the number of bits being in error during each second of the measurement.

Because of the delay introduced by the tested transmission link, the measurement process must be preceded by the synchronisation of the local test sequence generator in the receiver with the generator included in the transmitter. Details of this process are described in [4] and [6] and will not be discussed here.

It should be mentioned that the BER measurement must be performed on the formed, digital signal with clearly defined logical levels. In particular, the transmission clock is required to be either recovered or supplied externally to the receiver.

III. BER TESTER FOR 10 GB/S SYSTEM

The idea described in the previous section may be applied to the signal with any bit rate, at least in principle. However, at Gb-per-second data rates some special techniques and

Fig. 2. Simplified block diagram of 10 Gb/s BER tester.

Fig. 3. Structure of the single word of the test sequence.

Fig. 4. 10 Gb/s BERT transmitter.

modifications of the basic idea must often be used, according to the available technology. One of the most important things when designing the BER tester is the necessity to generate the serial data stream running with 10 Gb/s rate. Having no access to highly advanced technology of making integrated circuit, it is practically impossible to build a classical PRBS generator based on the serial shift register with feedback. This difficulty may be overcome by designing a generator and the error detector to operate on parallel words rather than on individual bits. Parallel data may then be easily converted into the serial stream by means of proper serialiser and deserialiser. This way the speed of the clock necessary to operate the tester may be reduced substantially. In the solution described herein, it was assumed at first that generation and further data processing would be performed with 622 MHz clock using Xilinx's Spartan3 FPGA (see Fig. 2). MAX3952/MAX3953 serialiser/deserialiser by Maxim are responsible for performing serial/parallel conversion.

Although some initial analysis suggested that it was possible to build BERT according to the diagram presented in Fig. 2, it turned out finally that full parallel architecture cannot be implemented in the Spartan3 device. Because of that, a modified and simplified architecture was developed, that fits into chosen FPGA circuit. The most important features of this architecture will be presented in the next chapters.

IV. TRANSMITTER WITH THE TEST SEQUENCES GENERATOR

The full parallel PRBS architecture (e.g. as described in [7]) proved to be too complex to operate with 622 MHz clock signal after implementation in Spartan3 FPGA. It was thus assumed that BER would be measured only on a few chosen bits (called the measurement channels) from the 16-bit parallel word. It was also taken that the transmitter would repeat each 16-bit sequence four times, which effectively lowers its clock speed to 155 MHz. This simplified greatly the test sequence generator.

The structure of the parallel words sent to the serialiser is presented in Fig. 3. Inside this word two bits, D8 and D15, have their values fixed to "zero" and "one", respectively. The BER of the link under test is determined based on these two bits only. The remaining 14 bits are divided into two unequal fields, with length 8 and 6 bits. These fields are filled
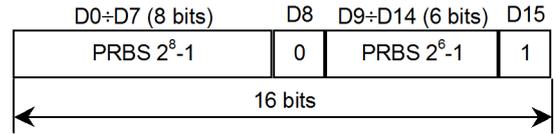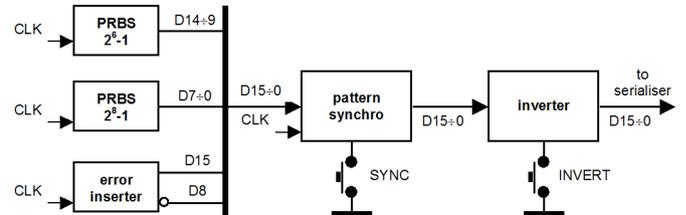
with PRBS having period $2^8 - 1$ and $2^6 - 1$, respectively. Such structure of the test word is justified by the requirement of having the serial data stream as "random" as possible, simultaneously preserving its DC balance. Because of different PRBS periods, the period of the resulting sequence is much longer than in the case of two PRBS with the same period.

The structure of the test word proposed herein posseses some shortcomings, however. The longest run of the same consecutive symbols is limited to 9 "ones" and 7 "zeros". It limits BERT capabilities when testing the immunity of transmission system to the low frequency spectral components contained in the signal. Further, the number of bits that could result in intersymbol interference (ISI) is also limited: for "one" there are 6 bits before and 8 bits after, for "zero" there is the reverse. These limitations, however, seem not to be a big problem, especially if the BERT is used to evaluate errors caused by fibre dispersion or laser chirp.

A complete BERT transmitter includes also a few additional blocks: pattern synchronisator, inverter and error inserter. The inverter is useful if the transmission link under test inverts the signal itself. This may be easily done even accidentally because I/O interfaces of the BERT use differential signaling. The error inserter allows for performing some kind of BERT self-test. If activated, it periodically changes the polarity of signals in the measurement channels for one clock period, thus forcing errors. Because the rate of these errors is known, it may be used to check for possible BERT or link under test malfunction. The pattern synchronization is necessary to align the bits at the output of the MAX3953 deserialiser with inputs of MAX3952 serialiser. When the deserialiser acquires serial synchronism with the data stream produced by the serialiser, the position of bits at its output is not necessarily correct. Thus, some kind of a barrel shifter, capable of the rotation of bits appearing at the output of the transmitter, is necessary to set the proper order of the bits. Although this circuit is associated rather with the deserialiser than serialiser, it appeared much easier to implement it inside the BERT transmitter.
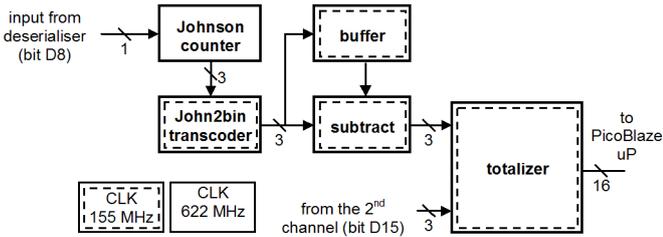
Fig. 5. 10 Gb/s BERT receiver.

V. BER DETECTOR AND ANALYSER

Because of the structure of the test word used in the presented design, the detection of errors is a straightforward task. To do this, it is enough to count the clock periods where the bits in the measurement channels differ from that set in the transmitter.

It is crucial for the BERT operation to run error counters at the clock speed equal to 622 MHz. To facilitate operation with such speed, the counting of errors is divided into a few tasks (see Fig. 5). At the input of each measurement channel a 3-bit fast counter is implemented. The Johnson's counters are used there because of their potential for high-speed operation. Simulations performed using ISE7 and ModelSim XE software packages (available form Xilinx and Mentor Graphics, respectively) showed that the counter composed of maximum of three D flip-flops (F/F) is capable to operate with required speed. The capacity of such Johnson counter equals 6. This allows the lowering of the clocking speed of the rest of the circuit four times (blocks operating with lower clock speed are marked with additional dashed border in Fig. 5). The counter used in the design is the synchronous one, with input from the measurement channel connected to the Clock Enable inputs of the F/F.

To obtain the number of bits being in error during the four consecutive clock cycles, it is necessary to calculate the difference between the current state of the Johnson's counter and its delayed state. To facilitate this operation, the output from the counter is converted into the natural binary format. After subtraction, the partial results are totaled in the 16-bit binary counter. The totalizer has two 3-bit inputs, one for each measurement channel (processing the circuitry for one channel only is shown in Fig. 5).

VI. EDITORIAL POLICY

After totaling the errors, the result is passed to the software PicoBlaze [8] processor implemented in the FPGA. This processor is responsible for calculating BER, displaying the result and communicating with the user.

BER calculation is made according to the formula similar to that given in equation (2):

$$BER = \frac{L}{N_A} \frac{1}{B} \frac{n_e}{\Delta t}, \qquad (3)$$

where L is the length of the parallel word and N_A is the number of channels measuring BER. Modification of the basic formula (2) results from the fact that BERT described in the

paper does not count all errors occurring during the transmission. It rather samples errors that degrade transmission on two chosen bits only. Taking the assumption that the probability of errors affecting the rest of bits is the same and that errors are independent, one may correct the result by simply increasing the error rate, as it is done in equation (3).

In our case $L = 16$, $N_A = 2$, $B = 10 \cdot 10^9$ and Δt was chosen to be measured in seconds. Putting all these numbers into equation (3), it may be simplified as:

$$BER = \frac{4}{5} \frac{n_e}{\Delta t} 10^{-9}. \qquad (4)$$

Using equation (4), BER may be quite easily calculated because all required mathematical operations are performed with the natural numbers. Multiplication by 4 in the numerator may be carried out by the logical left shift of n_e by two positions, whereas multiplication by 5 in the denominator requires two shifts and one more addition. The division operation must be performed having in mind a possibly very wide, being in orders of magnitude, dynamic range of the result. However, because there is a lot of time to obtain the result (1 second), the entire operation may be executed without resorting to the full floating point arithmetic. A simple procedure implemented in the design, exploits only multiplication by 10 and subtraction and allows calculate BER directly in the decimal $x.xx \cdot 10^{-y}$ format. The code for this procedure realized in 24-bit precision occupies about 150 PicoBlaze assembler instructions and executes in a small fraction of second.

VII. EXPERIMENTAL RESULTS

Using the BERT described above, some experimental data were taken in links operating with 10 Gb/s transmission speed. The results are presented in Fig. 6.

In Fig. 6a BER measured in the link composed of the laser transmitter followed by erbium doped fibre amplifier (EDFA) booster and 40 km of the standard singlemode fibre (SSM) is presented. The two curves are plotted for two different values of EDFA gain. Based on the plot, the power penalty may be determined. For the case presented this penalty is quite independent of the input power and is about -2 dB. The negative value of the penalty results probably from a constructive interaction of fibre nonlinearity/dispersion with the chirp of directly modulated laser.

When performing BER measurements, some care must be taken, however. In Fig. 6b the results of back-to-back BER measurement with neither fibre nor EDFA inserted between the transmitter and the receiver are presented. Two different results were obtained in exactly the same experimental setup. Between two measurements, only the connector in the optical path was disconnected and connected again. The difference is probably caused by the light backreflected from the connector to the laser. This generates some noise in the laser that strongly depends on the quality of the optical connection. This is evident, thus, that any conclusions concerning the penalties in the order of 1 dB should be drawn very carefully. It would be best to perform measurements a few times, observing the consistence of the results.
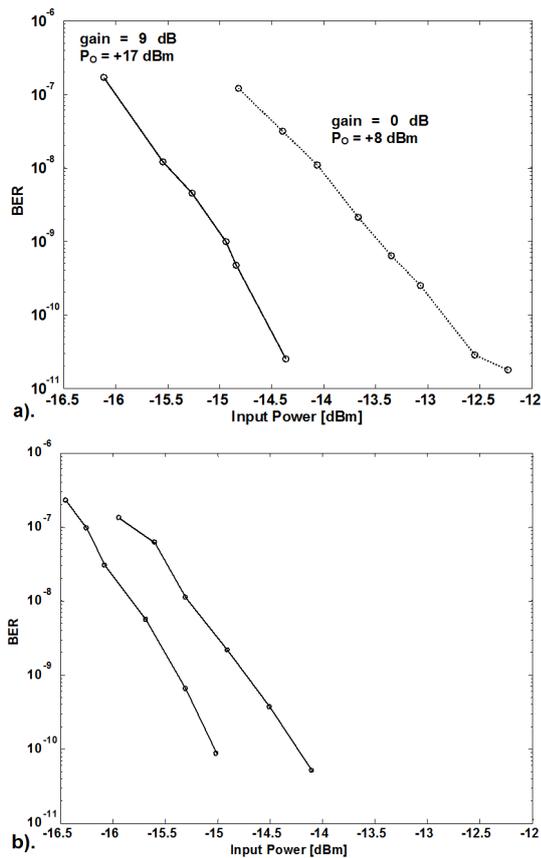
Fig. 6.   BER versus received optical power in a few experimental setups –desription in the text.

VIII. CONCLUSION

The bit error rate tester designed for operation in 10 Gb/s fibre optic links is described in the paper. The main purpose of this BERT was to evaluate the degradation of the signal quality, caused by a interaction of directly modulated laser chirp with fibre dispersion. This, however, does not limit the applications of the BERT to these cases only.

The architecture of the BERT described herein was tailored to the abilities of Spartan3 FPGA, that is used to implement most of the design. The usual operating idea of the BERT was found to be unsuitable for the design, therefore some special solutions were proposed. Using high-speed SiGe serialiser/deserialiser and exploiting extensively parallel architecture with pipelining, it was possible to overcome inherent speed limits of Spartan3 FPGA and build functional BERT operating at 10 Gb/s data rate.

The tester built according to the idea presented in the paper was tested in the laboratory and proved its usefulness for research and investigation purposes. The design lacks some features, however, that should be added in the next version. Because BER measurements are relatively time-consuming, it would be very helpful to log past values of BER for further analysis. This way, it would be possible to tell if the measured BER is inherent for the system under test, or if it was caused by some external interference. In addition, the capacity of the totalizer (16 bits) proved to be too small and should be extended to 24 bits.

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